INTEL® SPECIFICATION ADDENDUM FOR THE JEDEC DDR200/266 Un-buffered DIMM SPECIFICATION

Rev. 0.9
May 01, 2001

Intel Corporation

Table of Contents

Revision History (starting from Rev 0.7)

Revision Info	Page of Revision	Description of Change
0.9	8	Net Structure Routing & trace lengths for Address and Control (Raw Card Version C)
0.8	4, 5, 6, 7 and 8	All references were updated to Rev1.0 version of the JEDEC Spec
	4	184-pin DDR SDRAM DIMM Pin Assignments: Updated to reflect JEDEC ballot
	7	Location of ECC pin corrected
0.7	4	Input/Output functional description: Specified voltage range for V_{DDSPD}
	4	184-Pin DDR SDRAM DIMM Pin Assignments: Swapped pin A13 with FETEN
	4	Logical Clock Net Structures: Specified resistor and capacitor tolerances and added a note indicating that the 5 dram load case is not used
	4	Trace Lengths for clock net structures: Specified resistor tolerances and the value of the capacitors used.
	4	Trace Lengths for DQ, CVB and DQS Net Structures: Specified resistor tolerances
	5	Trace lengths for DM net structures: Specified resistor tolerances
	6	Net Structure Routing for Chip Select (Raw Card Version A): Specified the location of the ECC load
	7	Trace Lengths for Chip Select Net Structures (S0#, S1#): Corrected TL3 min/max values
	7	Net Structure Routing For Chip Select (Raw Card Version B): Specified location of ECC pin
	8	Net Structure Routing For Chip Select (Raw Card Version C): Specified location of ECC pin and updated missing label (TL5) from trace length at the bottom of the diagram.
	9	Serial Presence detect component specification: Specified requirement for write protecting the lower 128bytes of the SPD

Objective

This Specification addendum calls out changes to the JEDEC DDR SDRAM Unbuffered DIMM Design Specification Rev 1.0 (dated December 2000). The intent of this document is to clarify and detail specifications so as to create a more robust, cost effective, and compatible solution for DDR Memory.

Note: Page number references are to the JEDEC DDR SDRAM Unbuffered DIMM Design Specification Rev 1.0

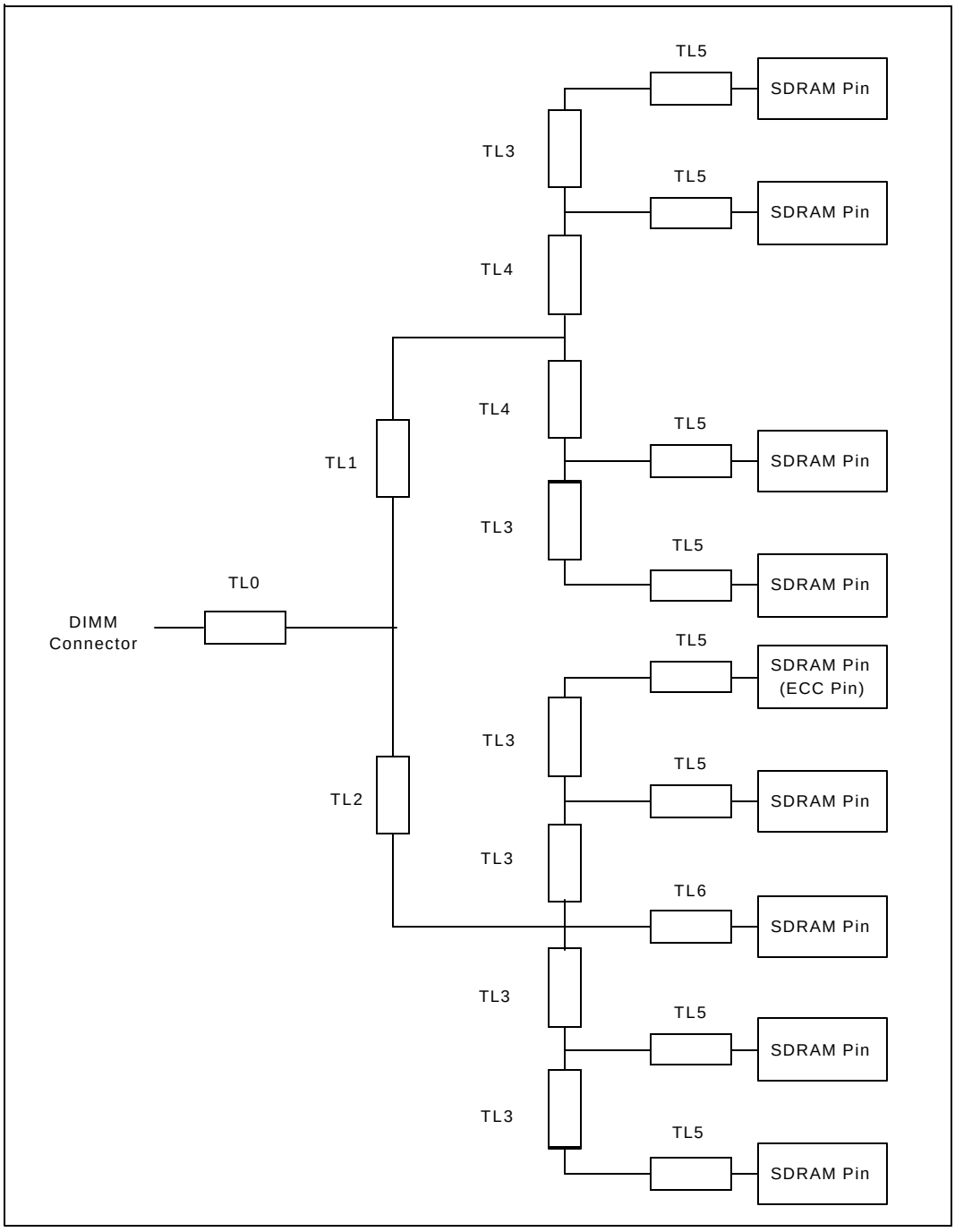
184-Pin DDR SDRAM DIMM Pin Assignments (page 7)

Pin #	X64 **Non-Parity**	**X72 ECC**
103	NC(FETEN)	NC(FETEN)
167	A13	A13

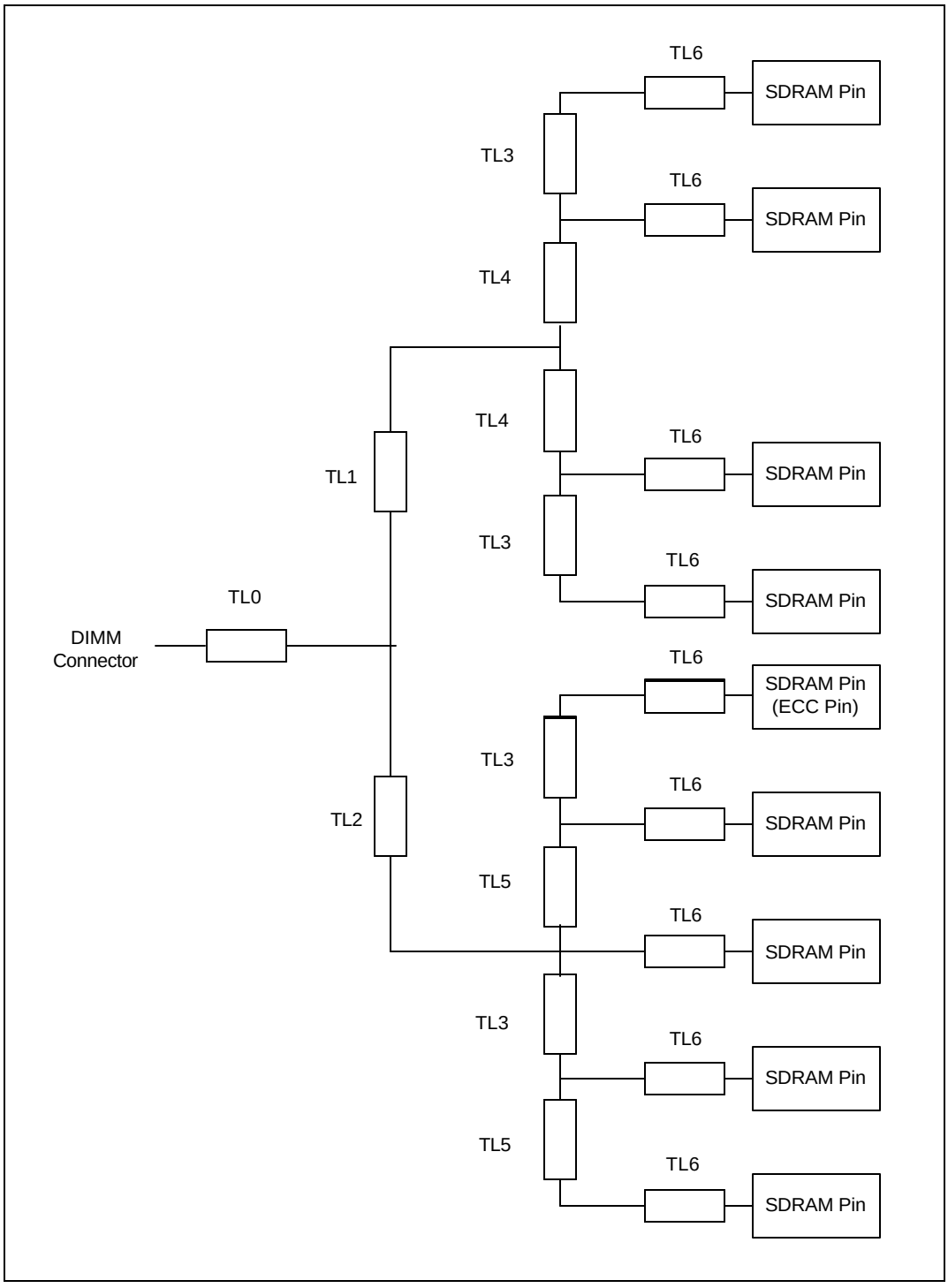
Logical Clock Net Structures (page 14)

Note3: The 5 DRAM load case is redundant and never utilized for Raw Cards A, B and C
Note4: The value of the capacitors used is 1.5pF

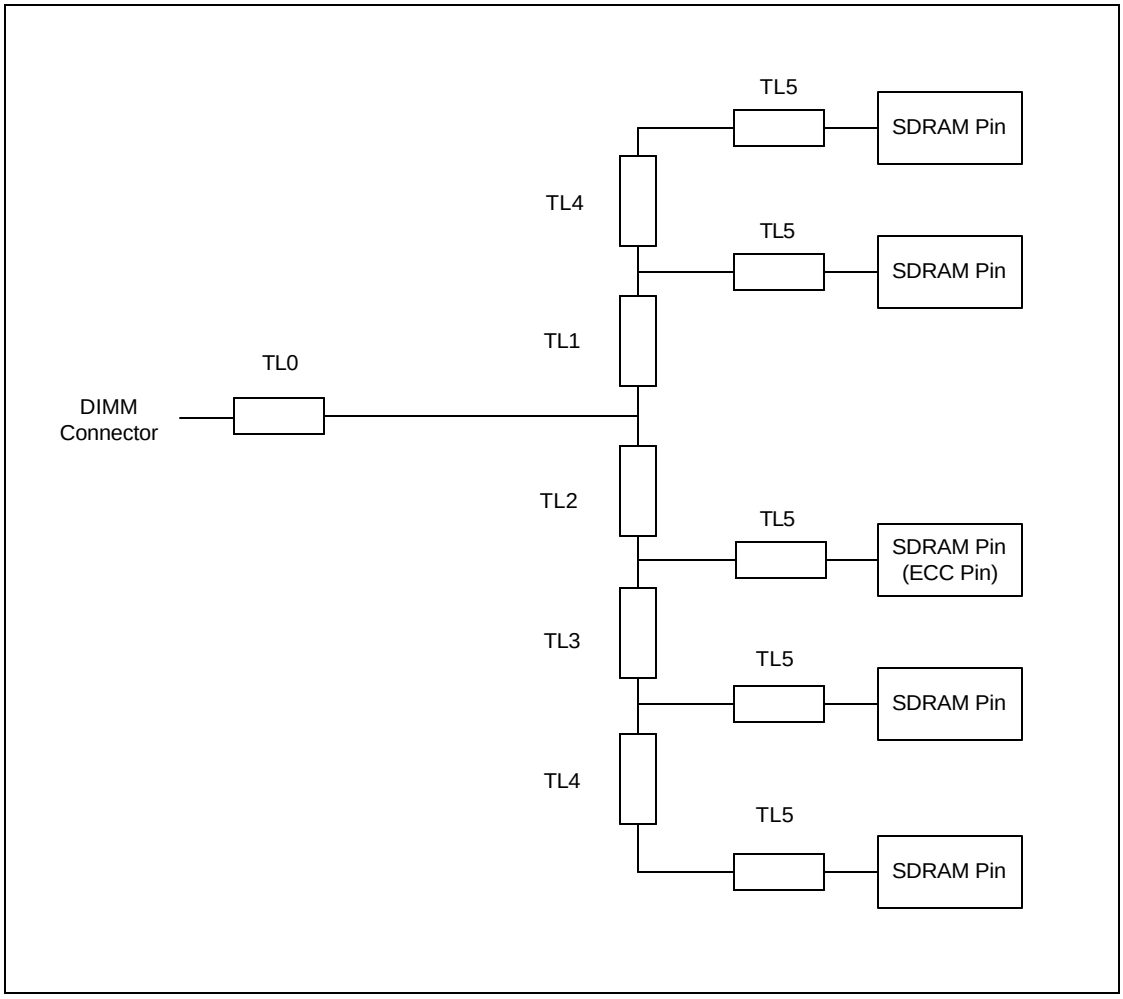
Net Structure Routing for Chip Select (Raw Card Version A) (Page 25)



Net Structure Routing for Chip Select (Raw Card Version B) (Page 26)

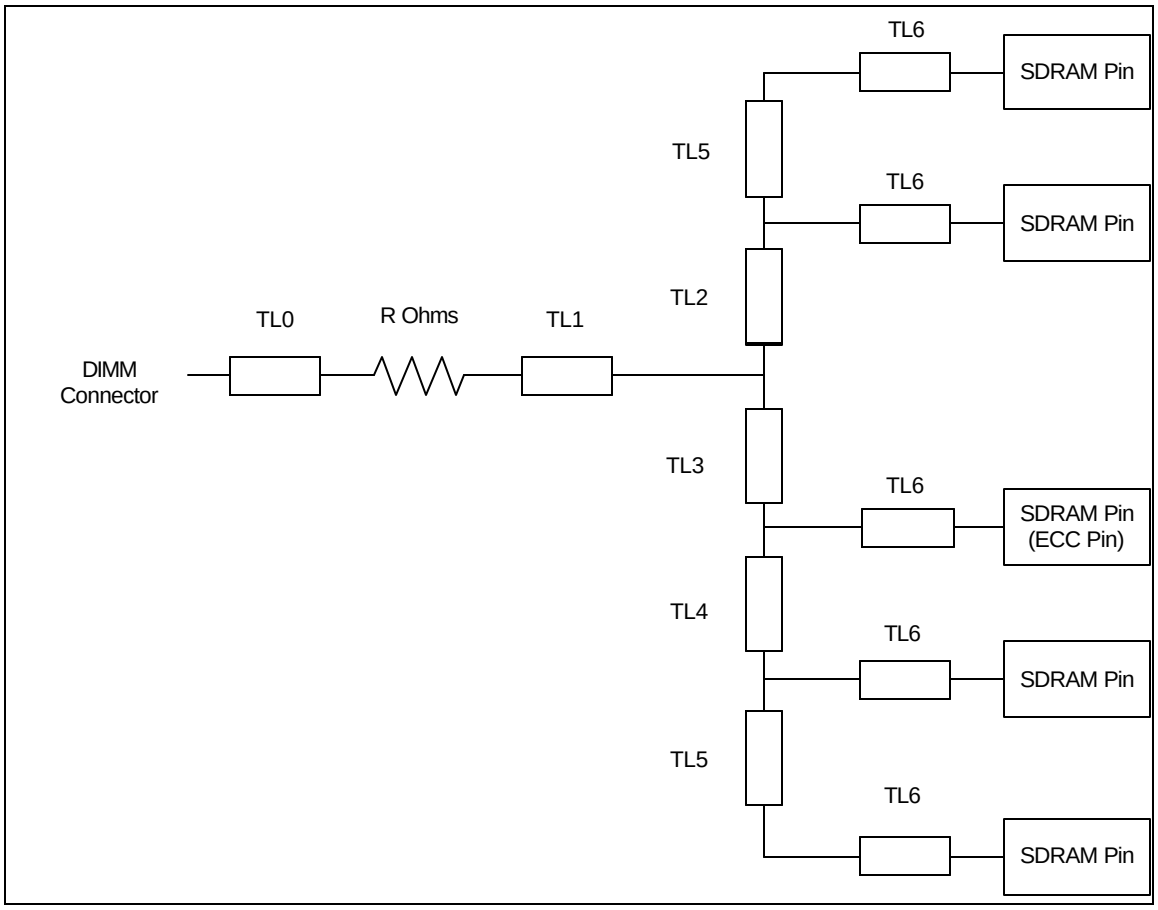


Net Structure Routing for Chip Select (Raw Card Version C) (Page 27)



Net Structure Routing for Address and Control (Raw Card Version C) (Page 33)

A, BA, /RAS, /CAS, /WE for Raw Card Version C



Trace Lengths for Address and Control Net Structures

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		R Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
C	.13	.30	5.28	5.60	.91	.92	.29	.30	.62	.63	.84	.85	.07	0.14	7.5 ± 5%	1,2

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches
2. The sum of TL0 + TL1 must be greater than 5.58 inches and less than 5.77 inches

Serial Presence Detect Component Specification (new)

The DIMM vendor should ensure that the lower 128 bytes can be software write protected. A write to the SPD with address "0 1 1 0 SA2 SA1 SA0 0", where SA(2:0) are the SPD addresses on the DIMM connector, will prevent all future writes to the lower 128 bytes of the SPD. The software write protect feature is "write once", but should be done by the BIOS at each power up, to prevent corruption of the lower 128 bytes of the SPD.